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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KOMAKI et al.

Art Unit: 2815

Application No. 09/939,752

Examiner: J. Nguyen

Filed: August 28, 2001

Atty. Docket No. 024016-00014

For: FUNDAMENTAL CELL, SEMICONDUCTOR INTEGRATED DEVICE, WIRING METHOD AND WIRING APPARATUS

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

October 21, 2002

Sir:

In reply to the Office Action mailed June 21, 2002, the period for response being extended to October 21, 2002 by the attached Petition for Extension of Time, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace page 1, paragraph 2, beginning at line 15 with:

A semiconductor integrated circuit device of the gate array type and standard cell type is used so far, in which functional circuit blocks constituted of fundamental cells in a matrix structure are arranged. Fig. 12 shows a typical example of a fundamental cell 100. The fundamental cell 100 has therein a power supply voltage wiring VDD and ground potential wiring VSS, or so-called the power rails VDD and VSS in order to supply the power supply voltage VDD and ground potential VSS respectively to the fundamental cell 100. Connection terminals 2 and 3 are used for biasing N-type well region of a PMOS (P-channel metal oxide semiconductor) transistor and a P-type well